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|---|----------------------------------|
| CERTIFICATE OF MAILING<br>37 C.F.R. § 1.8   |                                  |
| I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below: |                                  |
| <u>10/1/02</u><br>Date  | <u>John C. Gint</u><br>Signature |

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:  
Dale E. Gulick

Serial No.: 10/045,117

Filed: November 1, 2001

For: MICROCOMPUTER BRIDGE FOR  
REMOTE MANAGEABILITY

Group Art Unit: 2152

Examiner: Mark Rinehart

Atty. Dkt. No.: 2000.051400/TT4028

INFORMATION DISCLOSURE STATEMENT

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Assistant Commissioner for Patents  
Washington, D.C. 20231

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Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

The present Information Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Assistant Commissioner is hereby authorized to deduct said fees from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2000.051400/TT4028.

Applicant respectfully requests that the listed documents be made of record in the present case.

Applicants additional request that the following co-pending patent applications also be considered in the present case:

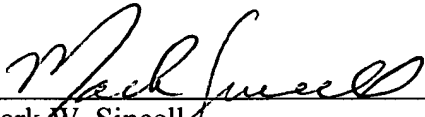
| <b>WMA NOS.</b> | <b>SERIAL NOS.</b> |
|-----------------|--------------------|
| 2000.038300     | 09/852,372         |
| 2000.038400     | 09/852,942         |
| 2000.038600     | 09/853,446         |
| 2000.038700     | 09/853,447         |
| 2000.038800     | 09/870,889         |
| 2000.038900     | 09/853,225         |
| 2000.039000     | 09/871,084         |
| 2000.039100     | 09/871,511         |
| 2000.039200     | 09/544,858         |
| 2000.039300     | 09/853,226         |
| 2000.039400     | 09/854,040         |
| 2000.039500     | 09/853,465         |
| 2000.039600     | 09/853,443         |
| 2000.039700     | 09/853,437         |
| 2000.063200     | 09/853,335         |
| 2000.080000     | 09/853,234         |
| 2000.080100     | 09/870,890         |
| 2000.051500     | 10/033,142         |
| 2000.051600     | 10/005,648         |
| 2000.051700     | 10/066,879         |
| 2000.051800     | 10/067,175         |
| 2000.051900     | 10/084,596         |

|             |            |
|-------------|------------|
| 2000.052000 | 10/066,948 |
| 2000.052100 | 10/023,233 |
| 2000.052200 | 10/044,707 |

Applicants submit herewith copies of these co-pending patent applications as required under 37 CFR 1.98(a)(2)(iii).

Applicants have listed the patent application serial numbers here instead of on the form PTO-1449 in accordance with the last paragraph of MPEP 609 (*i.e.* p. 600-133, 8<sup>th</sup> Ed., Aug. 2001) to avoid having serial numbers of pending applications printed on the face of an issued patent.

Respectfully submitted,

  
 Mark W. Sincell  
 Reg. No. 52,226

WILLIAMS, MORGAN & AMERSON  
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Date: October 1, 2002

Form PTO-1449 (modified)

Atty. Docket No.  
2000.051400/TT4028Serial N .  
10/045,117

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Applicant  
DALE E. GULICKFiling Date:  
November 1, 2001Group:  
2152

U.S. Patent Documents

See Page 1

Foreign Patent Documents

See Page 1

Other Art

See Page 1

## U.S. Patent Documents

| Exam. Init. | Ref. Des. | Document Number | Date | Name | Class | Sub Class | Filing Date of App. |
|-------------|-----------|-----------------|------|------|-------|-----------|---------------------|
|             | A1        |                 |      |      |       |           |                     |
|             | A2        |                 |      |      |       |           |                     |
|             | A3        |                 |      |      |       |           |                     |
|             | A4        |                 |      |      |       |           |                     |
|             | A5        |                 |      |      |       |           |                     |

## Foreign Patent Documents

| Exam. Init. | Ref. Des. | Document Number | Date | Country | Class | Sub Class | Translation Yes/No |
|-------------|-----------|-----------------|------|---------|-------|-----------|--------------------|
|             | B1        |                 |      |         |       |           |                    |
|             | B2        |                 |      |         |       |           |                    |
|             | B3        |                 |      |         |       |           |                    |
|             | B4        |                 |      |         |       |           |                    |
|             | B5        |                 |      |         |       |           |                    |

## Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

| Exam. Init. | Ref. Des. | Citation   |
|-------------|-----------|--|
|             | C1        | Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)   |
|             | C2        | Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99) |
|             | C3        | Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)   |
|             | C4        | FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)                                    |
|             | C5        | "Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, 203 - 212   |

EXAMINER:

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EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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U.S. Patent Documents  
See Page 1Foreign Patent Documents  
See Page 1Other Art  
See Page 1**Other Art (Including Author, Title, Date Pertinent Pages, Etc.)**

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|             | C7        | Intel, "Advanced Configuration and Power Interface Specification," Revision 1.0b, 02/02/1999   |
|             | C8        | Intel, "Advanced Configuration and Power Interface Specification," Revision 2.0, 07/27/2000  |
|             | C9        | Intel, "Advanced Configuration and Power Interface Specification," Revision 2.0 Errata, Errata Document Rev. 1.5, 04/13/2001   |
|             | C10       | Case, Fedor, Schoffstall, Davin, "A Simple Network Management Protocol (SNMP)" May, 1990   |
|             | C11       | "Network Device Class Power Management Reference Specification," Version 210, 10/12/2000 pp. 1-9   |
|             | C12       | Intel, "IPMI Intelligent Platform Management Interface Specification v 1.0," Document Revision 1.0, 09/16/1998   |
|             | C13       | Intel, "IPMI Intelligent Platform Management Interface Specification v 1.5," Document Revision 1.0, 02/21/2001   |
|             | C14       | Intel, "IPMI v 1.5 Addenda, Errata, and Clarifications – Intelligent Platform Management Interface Specification v1.5, revision 1.0," Addendum Document Revision 3, 05/16/2001 |
|             | C15       | Intel, "IPMI Platform Management FRU Information Storage Definition v1.0," Document Revision 1.0, 09/16/1998   |
|             | C16       | Socolofsky et al., "A TCP/IP Tutorial," January 1991   |
|             | C17       | Intel, "IMPI Platform Management FRU Information Storage Definition v1.0, Document Revision 1.1, 09/27/1999  |
|             | C18       | Intel, "Metolious ACPI/Manageability," Specification v1.0, 04/30/1999  |
|             | C19       | Intel, "IPMI Intelligent Platform Event Trap Format Specification v 1.0," Document Revision 1.0, 12/07/1998  |
|             | C20       | DMTF, "Common Information Model (CIM) Specification," DSP0004, Version 2.2, 06/14/1999   |
|             | C21       | Intel, "SMBus Control Method Interface Specification," Version 1.0, 12/10/1999   |

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*See Page 1*Foreign Patent Documents  
*See Page 1*Other Art  
*See Page 1*

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|             | C24       | Intel, "System Management Bus (SMBus) Specification," SBS Implementers Forum, Revision 2.0, 08/03/2000         |
|             | C25       | J. Postel, "User Datagram Protocol," ISI 08/28/1980  |
|             | C26       | "About the 8051 Microcontroller," pp. 1-16   |
|             | C27       | Intel, "8259A Programmable Interrupt Controller (8259A/8259A-2)," December, 1988                               |
|             | C28       | Intel, "Intel® 840 Chipset Platform Design Guide," October, 1999   |
|             | C29       | AMD, "AMD's AlterIT™ Technology for Advanced Systems Management," Publication No. 22297 Rev. A, December, 1998 |
|             | C30       | AMD, "AMD-766™ Peripheral Bus Controller Data Sheet," 23167B March, 2001                                       |

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